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Remarks:

Reconsideration of the application is respectfully requested.

Claims 1, 3, 4, 6, 7 and 9 are presently pending in the application. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In item 3 of the above-identified Office Action, claims 1, 3, 4, 6, 7 and 9 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,761,517 to Durham et al ("**DURHAM**") in view of U. S. Patent No. 5,943,203 TO Wang ("**WANG**").

Applicants respectfully traverse the above rejections.

More particularly, Applicants' claim 1 recites, among other limitations:

> a control device connected to said clock supply circuit and driving said clock supply circuit based upon the measured current consumption, **said control device providing a control signal to said control input of said pulse filter when said means for comparing determine that the instantaneous current consumption exceeds the definable threshold value**; and
>
> **said pulse filter suppressing an individual clock pulse of said clock signal generated by said clock signal generator, in response to said control signal at said control input**, such that said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock

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> frequency corresponding to a maximum permissible current consumption of the circuit. [emphasis added by Applicants]

Applicants' independent claims 4 and 7 recite similar limitations to those listed above from claim 1. As such, in all of Applicants' independent claims, **the pulse filter is directly controlled by the control signal** (i.e., **an individual pulse is filtered out whenever the control signal is provided** to the pulse filter, and **not filtered** out when the control signal is **not provided** to the pulse filter). The above limitations of Applicants' independent claims are neither taught, nor suggested, by the **DURHAM** and/or **WANG** references.

More particularly, pages 2 and 3 of the Office Action allege that **DURHAM** discloses the above limitations of Applicants' claims. Applicants respectfully disagree.

On page 2 of the Office Action, it is alleged that:

> Durham also teaches the pulse filter suppressing **individual clock pulses** (via 7) of the clock generator (27) **in response to the control signal** at the control input (from the control device). [emphasis added by Applicants]

Further, on page 3, the Office Action stated, in part, that Durham:

> . . .also teaches the pulse filter (1-7, 10-13, 20) **suppressing individual clock pulses** of the clock

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> generator (27), **when a high power condition is detected** (via sensor, 18), in response to the control signal at the pulse filter's control input (new_data of registers 10-13). [emphasis added by Applicants]

However, Applicants' independent claims clearly require the filter to **suppress an individual pulse, directly in response to the receipt of a control signal.** Contrary to Applicants' claimed pulse filter (which suppresses **an individual pulse, in response to each control signal**), col. 6 of **DURHAM**, lines 29 - 52, state:

> In the case where sensor 18 has determined that a high power condition exists, **the power$_{13}$ high signal** [A] **is provided to synchronization latches 14 and 15. Then, control state machine 16 receives a control signal** [B] **from latches 14 and 15 indicating the existence of the high power condition. Select signals** [C] **are then issued by state machine 16 to pattern generator 17 so that a bit pattern** [D] **corresponding to state level 3 can be provided by pattern generator 17. At this time, a 0111 bit pattern** [D] **output from pattern generator 17 and a 0010** [E] **is issued to the 4 bit shift register.** That is, a zero is input as the new_data in registers 10, 11 and 13. A logical one is input to register 12. The logical zero input to register 10 will cause a logical 1 to be output on the data_out port of register 10 and input to the old_data port of register 11. A logical 0 is then output to register 12 and a logical one is input to register 13 such that the logical zero is output from register 13 to AND gate 7. **It can be seen that the logical zero** [F] **will occur 25% of the time,** since 1 of the 4 bit characters causes a logical zero to be present at AND gate 7. Thus, for every fourth cycle, the active portion of the oscillator clock is negated and the system clock output on node 20 will run at an effective clock frequency of 75% of the oscillator clock. This is at state level 3. [emphasis and identifiers [A] - [F] added by Applicants]

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As such, it can be seen from the foregoing portion of **DURHAM**, that, in **DURHAM**, **a multitude of control signals** (marked as [A] - [F], by Applicants) are used to determine whether or not pulses will be suppressed by one of the shift registers. This is in contrast to Applicants' claimed invention reciting **one** control signal suppressing an individual pulse. In **DURHAM**, only the **power$_{13}$ high signal** [A] and the **control signal** [B] are indicative of a high power condition. However, neither the **power$_{13}$ high signal** [A] of **DURHAM**, nor the **control signal** [B] of **DURHAM**, **determines whether an individual pulse of the clock signal is filtered** by any of the shift registers of **DURHAM**. Rather, in **DURHAM**, the determination to filter pulses is made on the basis of the **logical zero signal** [F], which depends on **a number of inputs**, in particular the 0111 bit pattern [D] output from pattern generator 17 of **DURHAM** and a 0010 [E] is issued to the 4 bit shift register of **DURHAM**.

In particular, there are situations in the system of **DURHAM**, **where a high power condition is indicated, yet the current pulse is not filtered**. Inversely, in **DURHAM**, a pulse might be filtered, even if high power condition has **not** been indicated by a control signal.

In summary, in **DURHAM**, **the pulse filter OF DURHAM is not directly controlled** (i.e, "said pulse filter suppressing **an**

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individual clock pulse of said clock signal generated by said clock signal generator, **in response to said control signal**") by a control signal generated in response to a high power determination (i.e., the $power_{13}$ high signal [A] of **DURHAM**), as required by Applicants' claims.

Further, the **WANG** reference (cited in the Office Action as allegedly disclosing an instantaneous current sensor) does not cure the above-discussed deficiencies of the **DURHAM** reference. More particularly, like **DURHAM**, **WANG** fails to teach or suggest, among other limitations of Applicants' claims, a pulse filter with a control input, **which filters a single pulse of a clock signal in response to a control signal indicating that an instantaneous current consumption exceeds a definable threshold value.** As such, even the combination of **DURHAM** and **WANG** fails to teach or suggest all limitations of Applicants' independent claims.

Not only does the combination of **DURHAM** and **WANG** fail to teach Applicants' claimed invention, but also, the disclosure made in those references **specifically teach away** from Applicants' claimed invention. More particularly, the disclosure in **DURHAM** would specifically lead a person of ordinary skill in this art away from Applicants' claimed invention. For example, col. 2 of **DURHAM**, lines 1 - 5, state:

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> However, **if a power high condition occurs, the pattern generator alters its bit pattern output to the registers in order to incrementally reduce the frequency of the system clock signal**, being input to the clocked elements of the circuit. [emphasis added by Applicants]

As such, **DURHAM** discloses the use of a pattern generator and a loadable shift register, in order to incrementally throttle the clock frequency provided to an electronic circuit by means of a bit pattern output to the registers of the loadable shift register. In **DURHAM**, the bit pattern is generated by a state machine, which samples a power high signal. See, for example, col. 2 of **DURHAM**, lines 11 - 15.

As can best be seen in Figs. 2 and 4 of **DURHAM** the state machine of **DURHAM** and the loadable shift register of **DURHAM**, together, change the frequency provided to the electronic circuit **in a sequence of steps** (i.e., **incrementally**, as disclosed in col. 2 of **DURHAM**, lines 1 - 5), and **not instantaneously**. There is no way to combine the teachings of **DURHAM**, which teaches a **stateful or stepped**, and thus, a **persistent** system, with the teachings of **WANG** (i.e., in the manner suggested in the Office Action) so as to provide an **instantaneous** system, **without destroying the teachings of DURHAM**. Despite it being impermissible to combine two references, wherein the combination would destroy the teachings of those reference, such teachings also direct a

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person of ordinary skill in this art **away** from Applicants' claimed invention. In view of the teachings of **DURHAM** (i.e., a non-instantaneous adjustment), a person of ordinary skill in the art would not consider the use of an instantaneous current sensor to be of any benefit in the system of **DURHAM**.

As such, Applicants' claimed invention is believed to **not** be rendered obvious by the combination of **DURHAM** and **WANG**.

Further still, even if a person of ordinary skill in this art would, somehow, arguendo, replace sensor 18 of **DURHAM** with the instantaneous current sensor of **WANG** (as suggested in the Office Action), that person would **not** obtain Applicants' claimed invention. Rather, the combination of **DURHAM** and **WANG**, suggested in the Office Action, would result in a clock control system that would still be **stateful or stepped** (i.e., not an **instantaneous** system). In particular, under a combination of the teachings of **DURHAM** and **WANG**, a person of ordinary skill in the art would understand that, even if the input control signal A of **DURHAM** indicated a high power condition instantaneously, the output control signal F of **DURHAM** would not. Thus, the combination of **DURHAM** and **WANG** would not teach or suggest Applicants' claimed invention.

Further, Applicants maintain, and reiterate herein, the

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previous objection made to the statement in the previous Office Action, that a person of ordinary skill in the Art would combine **DURHAM** with **WANG**, as indicated in the Office Action dated December 6, 2006. Contrary to the allegations made in that Office Action, Applicants believe that the **WANG** reference is not pertinent to the particular problem with which the skilled person was concerned at the time the invention was made.

More particularly, one main problem at hand at the time the present invention was made, was to **provide a simple, yet effective, control mechanism for a frequency regulating circuit**. The **WANG** addresses **how to measure an instantaneous current consumption**. However, a person of ordinary skill in this art would not have known that, **by measuring an instantaneous current consumption**, a frequency **regulating** circuit, as provided, for example, in **DURHAM**, could be improved in order to provide an easier, more flexible frequency regulating circuit according to Applicants' presently claimed invention.

In view of the foregoing, it can be seen that Applicants' invention is patentable over the **DURHAM** and **WANG** references, whether taken alone, or in combination.

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It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1, 4 and 7. Claims 1, 4 and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 4 or 7.

In view of the foregoing, reconsideration and allowance of claims 1, 3, 4, 6, 7 and 9 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

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Respectfully submitted,

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